What is claimed is:

Claims:

1. A semiconductor structure comprising:

an active layer of a semiconductor material, said active layer including a strained region;

a substrate; and

an insulating layer disposed between said active layer and said substrate, said insulating layer containing a thickened region underlying said strained region, and said thickened region transferring tensile stress to said strained region.

2. The semiconductor structure of claim 1 wherein said insulating layer is a buried oxide layer and said active layer is silicon.

3. The semiconductor structure of claim 1 further comprising:

a source defined in said active layer;

a drain defined in said active layer; and

a channel defined in a portion of said active layer between said source and said drain, said channel disposed at least partially in said strained region of said active layer.

4. The semiconductor structure of claim 3 further comprising:

a gate electrode electrically isolated from said portion of said active layer defining said channel.

5. The semiconductor structure of claim 4 wherein said strained region divides said gate electrode.

6. The semiconductor structure of claim 4 wherein said gate electrode generally overlies said channel.

7. The semiconductor structure of claim 1 further comprising:
a semiconductor device fabricated using said active layer.

8. The semiconductor structure of claim 1 wherein said active layer is silicon and said thickened region of said insulating layer is formed by oxidation of said active layer.

9. The semiconductor structure of claim 9 wherein said insulating layer is silicon dioxide.

10. The semiconductor structure of claim 9 wherein said substrate is silicon and said thickened region is formed by oxidation of said substrate.

11. The semiconductor structure of claim 1 wherein said tensile stress is effective to enhance carrier mobility within said strained region.

12. The semiconductor structure of claim 1 wherein a thickness of said thickened region is increased by an increment in the range of about 5 nanometers to about 10 nanometers.

13. The semiconductor structure of claim 1 wherein said thickened region of said insulating layer has a thickness greater than that of surrounding regions of said insulating layer flanking said thickened region.

14. The semiconductor structure of claim 1 further comprising:
first and second anchors flanking said strained region, said first and second anchors effective for limiting relaxation of said strained region of said active layer.

15. The semiconductor structure of claim 16 wherein said first and second anchors comprise adjacent regions of said active layer flanking said strained region.

16. A method of fabricating a strained semiconductor structure, comprising:

selectively oxidizing an active layer locally at a location between the active layer and an underlying insulating layer so as to increase a thickness of the insulating layer across a thickened region, the thickened region inducing tensile stress in the active layer to thereby form a strained region in the active layer overlying the thickened region.

17. The method of claim 16 wherein the active layer is silicon, and selectively oxidizing the insulating layer comprises:

reacting the active layer with a gaseous oxidizing species diffusing in the insulating layer from an ambient environment to form the thickened region of the insulating layer.

18. The method of claim 17 wherein selectively oxidizing the insulating layer comprises:

covering the insulating layer and the active layer with an oxidation mask; and

forming windows in the oxidation mask that permit transport of a gaseous oxidizing species into the insulating layer for subsequent diffusion to the thickened region.

19. The method of claim 18 wherein covering the insulating layer and the active layer comprises:

forming a patterned layer of silicon nitride.

20. The method of claim 16 further comprising:

forming a source and a drain in the active layer, the source and the drain flanking a channel defined at least partially in the strained region of the active layer.

21. The method of claim 20 further comprising:

forming a gate electrode electrically isolated from the active layer and overlying the channel.

22. The method of claim 21 wherein the strained region divides the gate electrode.

23. The method of claim 16 further comprising:

selectively oxidizing a portion of a substrate supporting the insulating layer at a location underlying the strained region so as to increase the thickness of the overlying insulating layer in the thickened region.

24. The method of claim 23 wherein the insulating layer comprises silicon dioxide and the substrate comprises silicon.

25. The method of claim 16 wherein the insulating layer comprises silicon dioxide and the active layer comprises silicon.

26. A method of fabricating a strained semiconductor structure, comprising:

thickening a thickened region of an insulating layer at a location underlying a strained region of an active layer so as to induce tensile stress in the active layer and thereby form the strained region in the active layer.

27. The method of claim 26 wherein thickening the thickened region further comprises:

selectively oxidizing the active layer at an interface between the active layer and the insulating layer so as to locally increase a thickness of the thickened region.

28. The method of claim 27 wherein the active layer is silicon, and thickening the thickened region comprises:

reacting the active layer with a gaseous oxidizing species diffusing in the insulating layer from an ambient environment to a location beneath the strained region for forming the thickened region of the insulating layer.

29. The method of claim 28 wherein reacting the active layer comprises:

covering the insulating layer and the active layer with an oxidation mask; and

forming windows in the oxidation mask that permit transport of a gaseous oxidizing species into the insulating layer for subsequent diffusion.

30. The method of claim 29 wherein covering the insulating layer and the active layer comprises:

forming a patterned layer of silicon nitride.

31. The method of claim 26 further comprising:

forming a source and a drain in the active layer, the source and the drain flanking a channel defined at least partially in the strained region of the active layer.

32. The method of claim 31 further comprising:

forming a gate electrode electrically isolated from the active layer and overlying the channel.

33. The method of claim 32 wherein the strained region divides the gate electrode.

34. The method of claim 26 further comprising:

selectively oxidizing a substrate supporting the insulating layer at a location underlying the strained region so as to increase the thickness of the overlying insulating layer in the thickened region.